

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Fukutomi et al.	Confirmation No.:	
Serial No.:	To be assigned	Art Unit:	2813
Filed:	November 10, 2003	Examiner:	To be assigned
For:	FABRICATION PROCESS OF SEMICONDUCTOR PACKAGE AND SEMICONDUCTOR PACKAGE	Attorney Docket No.:	7426-083-999

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

Enclosures accompanying this Information Disclosure Statement are a list of all foreign patents, publications, applications, or other information submitted for consideration by the office and a legible copy of each publication or that portion which caused it to be listed on the PTO-1449;

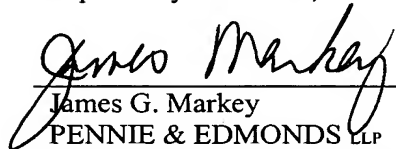
This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) before the mailing of an Office Action on its merits.

The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Pennie & Edmonds LLP Deposit Account No. 16-1150.

No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: November 10, 2003


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LIST OF REFERENCES CITED BY APPLICANT
(Use several sheets if necessary)

ATTY DOCKET NO. 7426-083-999	APPLICATION NO To be assigned
APPLICANT Fukutomi <i>et al.</i>	
FILING DATE November 10, 2003	GROUP To be assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLA SS	FILING DATE IF APPROPRIATE
	A01	5,579,207	11/01/96	Hayden <i>et al.</i>			
	A02	5,467,252	11/01/95	Nomi <i>et al.</i>			
	A03	5,399,903	03/21/95	Rostoker <i>et al.</i>			
	A04	5,381,039	01/01/95	Morrison			
	A05	5,216,278	06/01/93	Lin <i>et al.</i>			
	A06	5,173,766	12/22/92	Long <i>et al.</i>			
	A07	4,975,765	12/04/90	Ackermann <i>et al.</i>			
	A08	4,688,150	08/18/87	Peterson			
	A09	4,376,287	03/01/83	Sechi			
	A10	3,878,555	04/01/75	Freitag <i>et al.</i>			
	A11	3,748,543	07/01/73	Roberson			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	A12	JP 6053383	02/25/94	JAPAN			X	
	A13	JP 5-129473	05/25/93	JAPAN			X	
	A14	WO 92/21150	11/26/92	PCT			X	
	A15	JP 4277636	10/02/92	JAPAN			X	
	A16	JP 4072658	03/06/92	JAPAN			X	
	A17	JP 4-26545	03/03/92	JAPAN				
	A18	JP 3094459	04/19/91	JAPAN			X	
	A19	JP 3094430	04/19/91	JAPAN			X	
	A20	WO 90/13991	11/15/90	PCT/US90/01828				
	A21	EP 0391790 A1	10/10/90	EUROPE				
	A22	JP 2153542	06/13/90	JAPAN			X	
	A23	JP 1289273	11/21/89	JAPAN			X	
	A24	JP 61222151	10/02/86	JAPAN			X	
	A25	JP 60160624	08/22/85	JAPAN			X	
	A26	JP 59231825	12/26/84	JAPAN			X	
	A27	59-208756	11/27/84	JAPAN			X	
	A28	JP 59043554	03/10/84	JAPAN			X	
	A29	EP 0 091 072 A	10/12/83	EUROPE				

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	A30	Matsuo <i>et al.</i> , "Smallest Flip-Chip-Like Package 'Chip Scale Package (CSP)", The Second VLS Packaging Workshop of Japan 1994
	A31	Nikkei Materials & Technology 94.4 (No. 140)
	A32	Tummala <i>et al.</i> ; Microelectronics Packaging Handbook: Semiconductor Packaging Second Edition Part II

EXAMINER**DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.